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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/848,175	05/03/2001	Sang Hoo Dhong	AUS920010087US1	7651
35236	7590	06/10/2005	EXAMINER	
THE CULBERTSON GROUP, P.C. 1114 LOST CREEK BLVD. SUITE 420 AUSTIN, TX 78746			WILSON, ROBERT W	
			ART UNIT	PAPER NUMBER
			2661	

DATE MAILED: 06/10/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

# Office Action Summary

Application No.

09/848,175

Applicant(s)

DHONG ET AL.

Examiner

Robert W. Wilson

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

## Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

## Status

- 1) ☒ Responsive to communication(s) filed on 16 May 2005.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

## Disposition of Claims

- 4) ☒ Claim(s) 1-24 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 18-24 is/are allowed.
- 6) ☒ Claim(s) 1-6, 8-11 and 13-16 is/are rejected.
- 7) ☒ Claim(s) 7, 12 and 17 is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

## Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

## Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

## Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)  
Paper No(s)/Mail Date \_\_\_\_\_
- 4) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date. \_\_\_\_\_
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: \_\_\_\_\_

  
PHIRIN SAM  
PRIMARY EXAMINER

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### DETAILED ACTION

1.0 The application of Dhong et. al. entitled COMMUNICATION BUS WITH REDUNDANT SIGNAL PATHS AND METHOD FOR COMPENSATING FOR SIGNAL PATH ERRORS IN A COMMUNICATION BUS filed on 5/3/2001 and amended on 5/16/05 was examined. Claims 1-24 are pending.

#### *Claim Rejections - 35 USC § 103*

2.0 The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 1-5, 8-11, 13-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Atac (U.S. Patent No.: 4,985,830) in view of Nakamura (U.S. Patent No.: 4,982,114).

Referring to Claim 1, The Atac teaches: a source node (PROCESSOR) connected via a source switching arrangement (BUS SWITCH) which is connected via alternate transmission paths (plurality of BRANCH BUS paths) to a destination switch (Another BUS SWITCH) to a destination node (Another PROCESSOR) per Fig. 1.

The reference teaches that the BUS SWITCH is a card that is connected to the back plane per col. 2 lines 26-63

Atac does not expressly call for: a number of alternate paths between the source node and the destination node on a common substrate comprising a semiconductor but teaches number of alternate paths on a back plane per col. 2 lines 26-63

Nakamura teaches: interconnection lines or alternate paths between bus switches on a semiconductor substrate surface or a number of alternate paths between the source node and the destination node on a common substrate comprising a semiconductor per col. 8 lines 1-51.

It would have been obvious to one of ordinary skill in the art at the time of the invention add the integration of bus switches and interconnecting lines of Nakamura on a semiconductor substrate in place of the bus switches and bus of Atac in order to utilize less space to perform the same function.

In addition Atac teaches:

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Regarding Claim 2, There are multiple BUS SWITCHES (Source Switching devices) connected to different processors (Source node) via a plurality of BRANCH BUS (Alternate path) per Fig 1. A destination BUS SWITCH is connected to a destination processor per Fig 1.

Regarding Claim 3, A BUS SWITCH (source switching device) performs as a multiplexer and another BUS SWITCH (destination switching device) performs as a multiplexer per Fig 1.

Regarding Claim 4, A BUS SWITCH (source switching device) performs as a switch control structure and another BUS SWITCH (destination switching device) performs as a switch control structure per Fig 1.

Regarding Claim 5, The BUS SWITCH performs the switch control function. A BUS SWITCH is inherently controlled by a BUS SWITCH CONTROLLER and a BUS SWITCH CONTROLLER is a processor which inherently contains memory.

Regarding Claim 8, a plurality source PROCESSORS which are source and additional processors and a plurality of destination processors which are destination and additional processor with a plurality of BRANCH BUS connections between the source processor and additional source processor and destination and additional destination PROCESSORS (plurality of ALTERNATE paths). The BUS SWITCH which performs source switch arrangement and a BUS SWITCH which performs destination switch arrangement that can selectively connect and disconnect between the plurality of BRANCH BUS in order to provide transmission paths per Fig 1.

Regarding Claim 9, a BUS SWITCH performs a source switching arrangement multiplexing function per Fig 1. Atac does not expressly call for: source switching arrangement comprising a number of multiplexers but teaches multiplexing between a plurality of PROCESSORS per Fig 1. It would have been an obvious to one of ordinary skill in the art at the time of the invention for the BUS SWITCH to comprise a number of multiplexers in order for the BUS SWITCH to multiplex between a plurality of PROCESSORS.

Regarding Claim 10, A plurality of PROCESSORS or source nodes are connected side by side to the BUS SWITCH which is a common multiplexer as shown in Fig 1.

Regarding Claim 11, the plurality of BRANCH BUS can be divided up into subsets of alternate paths per Fig 1.

Referring to Claim 13, The Atac teaches: a plurality of PROCESSORS (source nodes) are connected via a plurality of BRANCH BUS (communications bus) to a plurality of PROCESSOR (destination nodes) per Fig 1. There are a plurality of BRANCH BUS to provide alternate paths. The BUS switch performs the source switching arrangement and another BUS SWITCH performs a destination switch arrangement as shown in Fig 1. The BRANCH BUS provide a number of alternate transmission paths extending between each PROCESSOR

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(Source) and a matched destination node (PROCESSOR). The BUS SWITCHs set up a BRANCH BUS path which matches the PROCESSOR (source) to the PROCESSOR (destination) as shown per Fig 1. The reference teaches that the BUS SWITCH is a card that is connected to the back plane per col. 2 lines 26-63

Atac does not expressly call for: a number of alternate paths between the source node and the destination node on a common substrate comprising a semiconductor but teaches number of alternate paths on a back plane per col. 2 lines 26-63

Nakamura teaches: interconnection lines or alternate paths between bus switches on a semiconductor substrate surface or a number of alternate paths between the source node and the destination node on a common substrate comprising a semiconductor per col. 8 lines 1-51.

It would have been obvious to one of ordinary skill in the art at the time of the invention add the integration of bus switches and interconnecting lines of Nakamura on a semiconductor substrate in place of the bus switches and bus of Atac in order to utilize less space to perform the same function.

In addition Atac teaches:

Regarding Claim 14, a BUS SWITCH (source switching devices) performs as a multiplexer and another BUS SWITCH (destination switching device) performs as a multiplexer per Fig 1.

Regarding Claim 15, A plurality of PROCESSORs or source nodes are connected side by side to the BUS SWITCH which is a common multiplexer as shown in Fig 1.

Regarding Claim 16, the plurality of BRANCH BUS can be divided up into subsets of alternate paths per Fig 1.

### ***Claim Rejections - 35 USC § 103***

3.0 The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all

obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

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Claims 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Atac et. al. (U.S. Patent No. 4,985,830) in view of in view of Nakamura (U.S. Patent No.: 4,982,114) further in view of Sugawara (U.S. Patent No.: 6,185,706)

Referring to Claim 6, The combination of Atac and Nakamura teach: the communications bus of claim 1 and a source and destination node.

The combination of Atac and Nakamura do not expressly call for: applying a test signal to each alternate transmission path and for monitoring the destination node to determine whether the respective test signal is properly received at the destination node

Sugawara teaches: applying a test signal to each alternate transmission path and for monitoring the destination node to determine whether the respective test signal is properly received at the destination node  
Col. 3 lines 30-61

It would have been obvious to one of ordinary skill in the art at the time of the invention to add the testing of Sugawara to the integrated circuit of the combination of Atac and Nakamura in order test the circuitry of the integrated circuit as part of quality control testing.

### ***Claim Objections***

4.0 Claims 7, 12, & 17 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

### ***Allowable Subject Matter***

5.0 The present invention is directed to a communication device for testing of alternate transmission paths on a bus between a source node and destination node which is on a common substrate. A test signal is applied to one of the paths between the source node and destination node and if the signal is not properly received at the destination node then switching to the alternate path.

The closest prior art are Sugawara (U.S. Patent No.: 6,185,706) and Yung (U.S. Patent No.: 4,970,724). Sugawara teaches testing all signal paths between source and destination nodes with a tester and then evaluating whether the values from all of the alternate paths falls to determine whether they are within specification. Yung teaches testing of redundant functional

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circuit modules on a wafer in order to determine which circuit modules can be connected together in order to determine a functioning circuit.

The closest prior art does not disclose either singularly or in combination disclose, anticipate or render obvious the following claim limitation: “applying a test signal to a first one of the alternate transmission paths between the source node and the destination node; determining whether the test signal is properly received at the destination node; and **if the test signal is not properly received at the destination node, switching to a second one of the alternate transmission paths between the source node and destination node.**” as claimed in claim 18.

In addition:

Claims 19-22 are allowable because they depend upon claim 18.

The present invention is directed to device which has a communication source and destination node in which there are a number of alternate paths between the nodes and destination nodes. The device is on a common substrate. The device has a source switching arrangement, a destination switching arrangement, and test circuitry which starts testing upon initialization of the communication bus.

The closest prior art is Atac (U.S. Patent No.: 4,985,830), Nakamura (U.S. Patent No.: 4,982,114), and Sugawara (U.S. Patent No.: 6,185,706). Atac teaches a device which has a communication source and destination node in which a number of alternate paths between the nodes are controlled by a source switching and destination switching devices which are interconnected via a backplane. Nakamura teaches integration of the source node switching and destination node switching device and bus on a common substrate. Sugawara teaches testing all signal paths between source and destination nodes with a tester and then evaluating whether the values from all of the alternate paths falls within a range of values and if so then the integrated circuit is assumed to be within the specification.

The closest prior art does not disclose either singularly or in combination disclose, anticipate or render obvious the following claim limitations: “test circuitry connected to the source node and destination node for applying a test signal to each alternate transmission path **at initialization** of the communication bus and for monitoring the destination node to determine whether the respective test signal is properly received at the destination node” as claimed in claim 23.

In addition:

Claim 24 is allowed because it depends upon claim 23.

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***Response to Amendment***

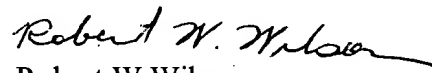
6.0 Applicant's arguments with respect to claims 1-24 have been considered but are moot in view of the new ground(s) of rejection. Please refer to the above rejection for details.

***Conclusion***

7.0 Any inquiry concerning this communication or earlier communications from the examiner should be directed to Robert W Wilson whose telephone number is 571/272-3075. The examiner can normally be reached on M-F (8:00-4:30).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chau T. Nguyen can be reached on 571/272-3126. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

  
Robert W Wilson  
Examiner  
Art Unit 2661

RWW  
May 31, 2005

  
**PHIRIN SAM  
PRIMARY EXAMINER**